WHAT IS CLAIMED IS:

1. A static random access memory device, comprising:

a first bias voltage contact biasable to a first potential;

a second bias voltage contact biasable to a second potential that differs from said first potential; and

a well having channels formed therein and connected to one of said first and second bias voltage contacts based on a transistor characteristic of said SRAM device that bears on static noise margin and write trip voltage.

2. The device as recited in Claim 1 further comprising a fuse circuit that connects said well to said one.

3. The device as recited in Claim 1 further comprising a conductor in an interconnect layer of said device that connects said well to said one based on a position of said conductor.

4. The device as recited in Claim 1 further comprising a bond pad that connects said well to said one.

5. The device as recited in Claim 1 wherein said device is couplable to a switch that connects said well to said one.

6. The device as recited in Claim 1 wherein said first potential is a chip supply voltage and said second potential is an input/output buffer supply voltage.

7. The device as recited in Claim 1 wherein a built-in self test system determines said one.

8. A method of manufacturing a static random access memory device, comprising:

providing a substrate;

forming in said substrate a well having a first dopant type;

forming in said well a transistor array including at least one channel having a second dopant type opposite said first dopant type;

determining a transistor characteristic of said transistor array that bears on static noise margin and write trip voltage; and

connecting said well to one of a first bias voltage contact biasable to a first potential or a second bias voltage contact biasable to a second potential based on said transistor characteristic.

9. The method as recited in Claim 8 wherein said connecting comprises connecting said well to said one with a fuse circuit of said device.

10. The method as recited in Claim 8 wherein said connecting comprises connecting said well to said one with a conductor in an interconnect layer of said device.

11. The method as recited in Claim 8 wherein said connecting comprises connecting said well to said one with a bond pad of said device.

12. The method as recited in Claim 8 wherein said connecting comprises connecting said well to said one with a switch coupled to said device.

13. The method as recited in Claim 8 wherein said first potential is a chip supply voltage and said second potential is an input/output buffer supply voltage.

14. The method as recited in Claim 8 further comprising determining said one with a built-in self test system.

15. A static random access memory device, comprising:

a substrate;

a well located in said substrate and having a first dopant type;

a transistor array located in said well and including channels having a second dopant type opposite said first dopant type;

a first bias voltage bus proximate said transistor array and biasable to a chip supply voltage; and

a second bias voltage bus proximate said transistor array and biasable to an input/output buffer supply voltage that differs from said chip supply voltage, a well having channels formed therein and connected to one of said first and second bias voltage contacts based on a transistor characteristic of said transistor array that bears on static noise margin and write trip voltage.

16. The device as recited in Claim 15 further comprising a fuse circuit that connects said well to said one.

17. The device as recited in Claim 15 further comprising a conductor in an interconnect layer of said device that connects said well to said one.

18. The device as recited in Claim 15 further comprising a bond pad that connects said well to said one.

19. The device as recited in Claim 15 wherein said device is couplable to a switch that connects said well to said one.